

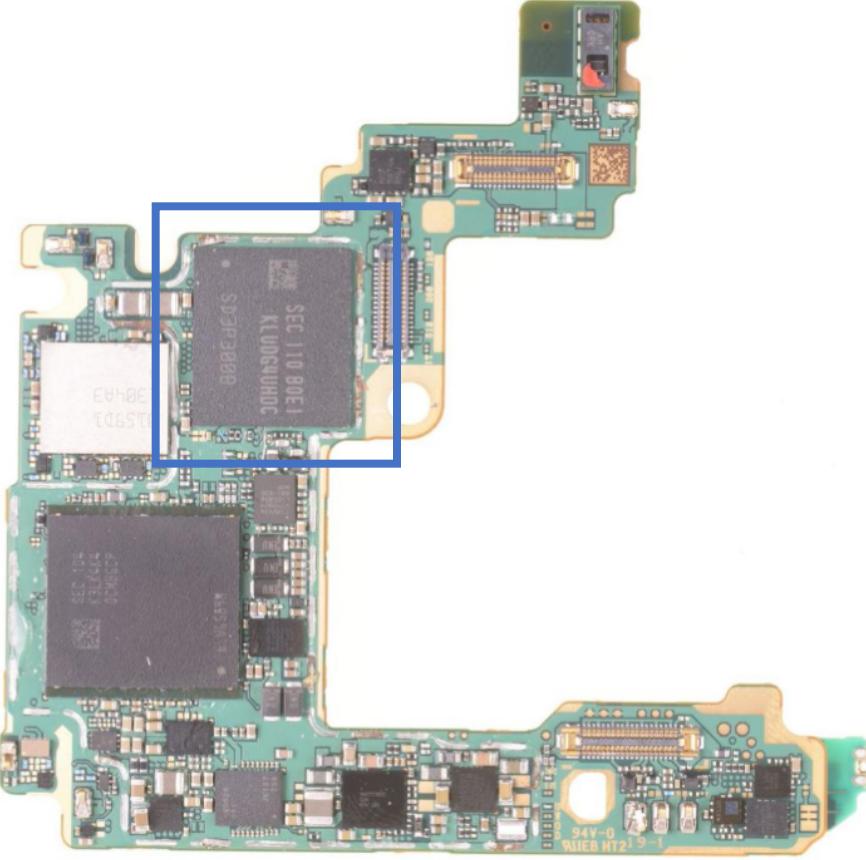
EXHIBIT I

U.S. Patent No. 6,724,241 (“241 Patent”)**Accused Products**

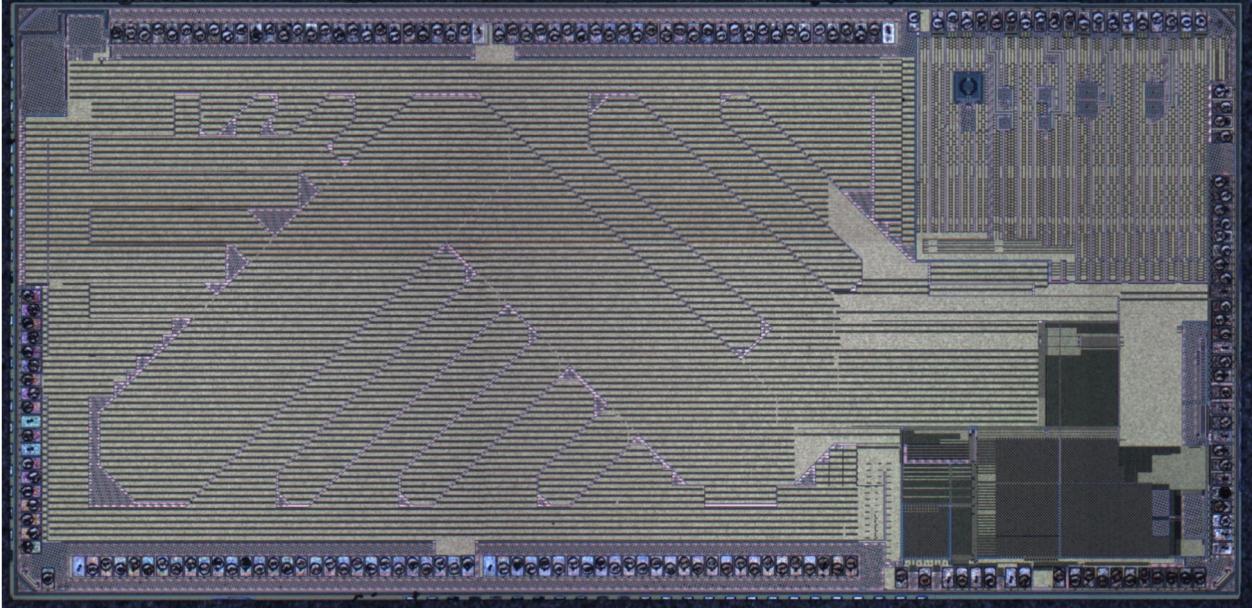
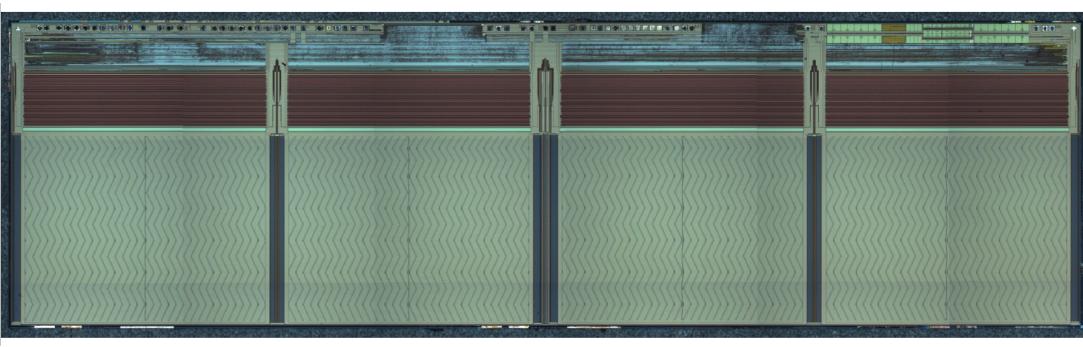
Samsung products with Samsung NAND flash chips, including without limitation the Samsung Galaxy S21 Ultra 5G (“Accused Products”), infringe at least Claims 1-3 and 6-8 of the ’241 Patent.

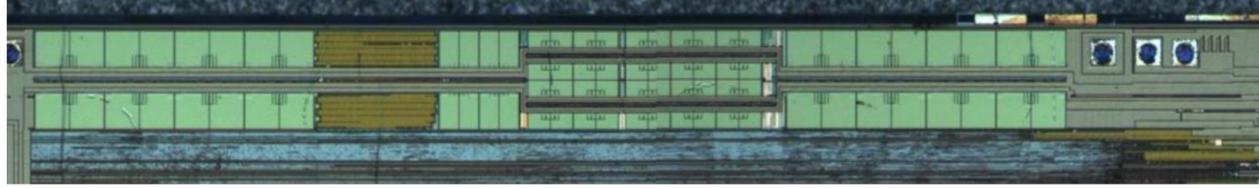
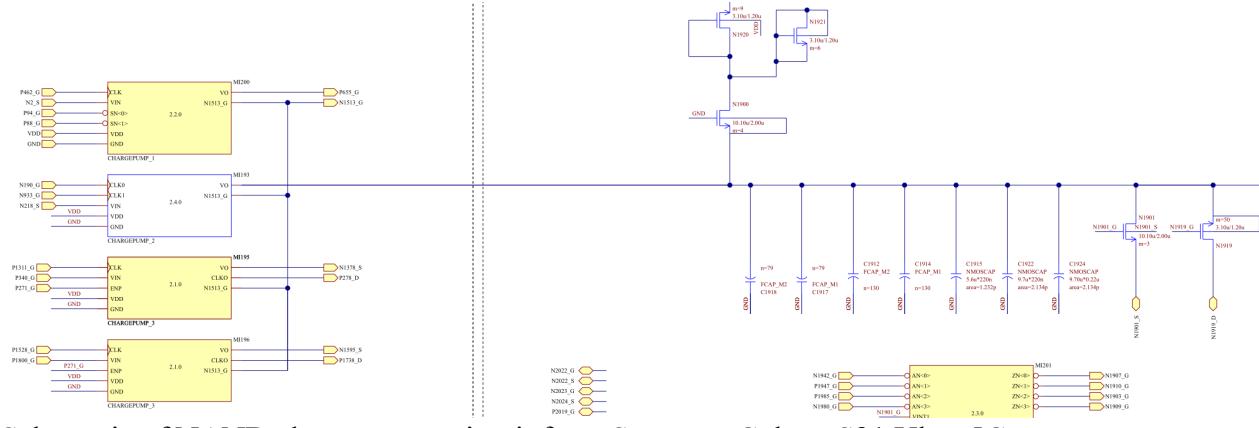
Claim 1

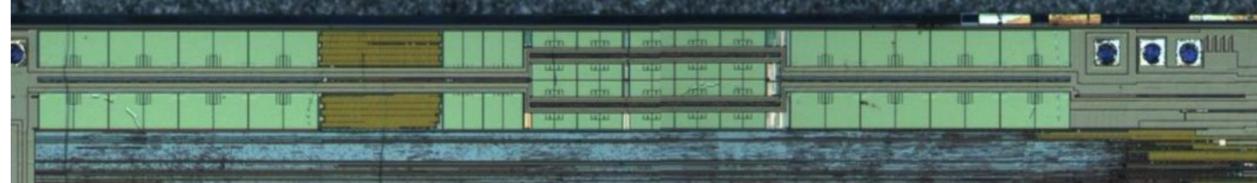
Claim 1	Accused Products
[1pre] 1. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	<p>To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.</p> <p>For example, the Samsung Galaxy S21 Ultra 5G includes the charge pump circuit of the Samsung NAND flash circuit, package marking SEC 110 BOE1 KLUDG4UHDC SD3P300B.</p> <p><i>See, e.g.:</i></p>

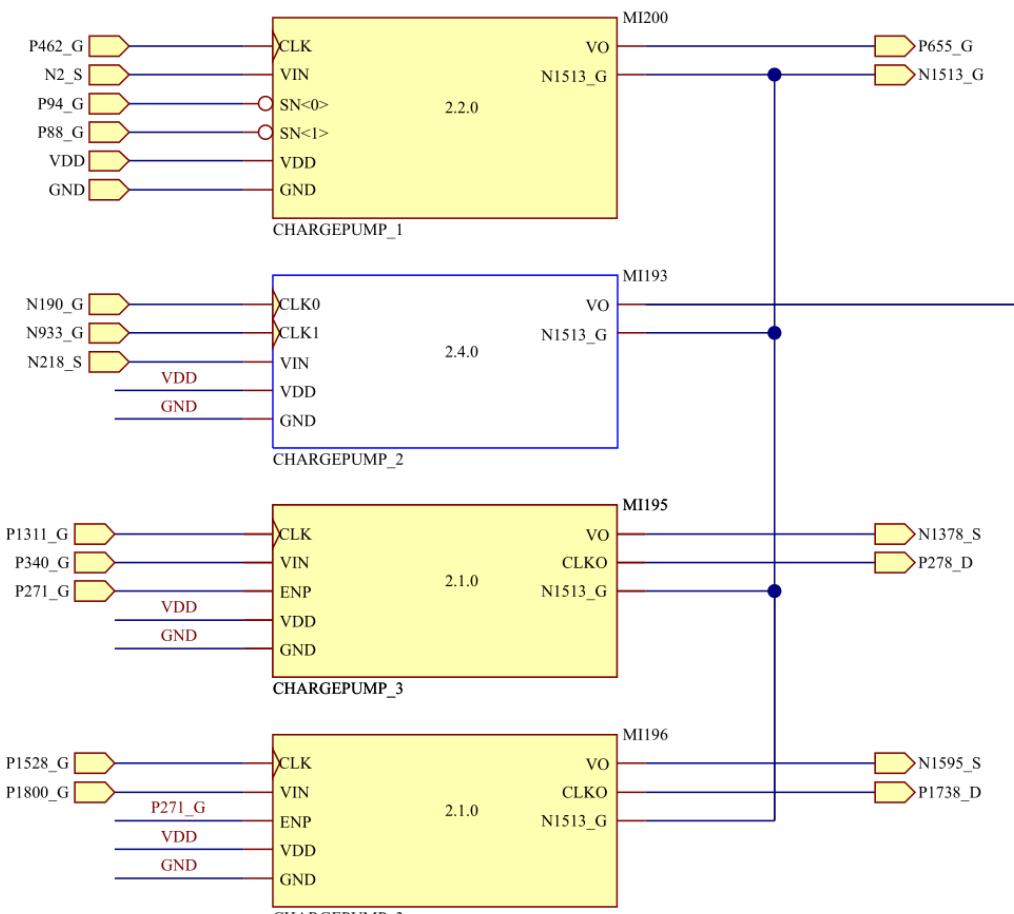
Claim 1	Accused Products
	 <p>Photograph of main system board from Samsung Galaxy S21 Ultra 5G, with NAND circuit indicated</p>

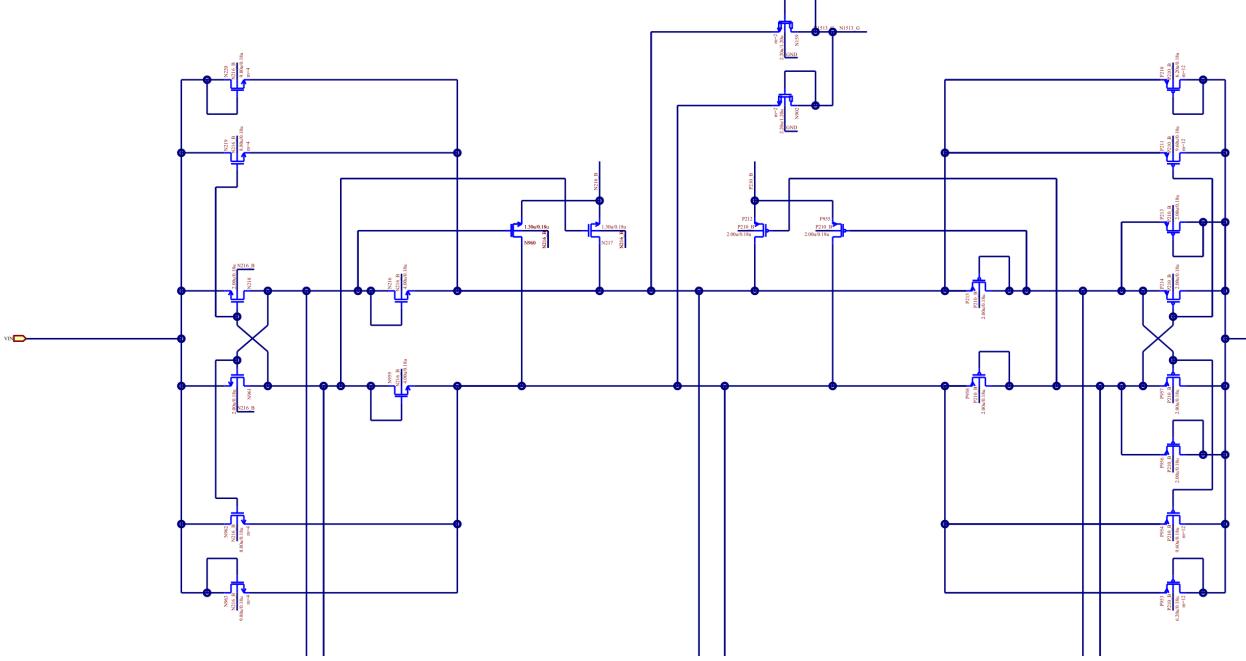
Claim 1	Accused Products
	 A close-up photograph of a NAND flash memory chip. The chip is dark grey with white text and a QR code. The text reads "SEC 110 BOE1" on the top line, "KLUDG4UHDC" on the second line, and "SD3P300B" on the bottom line. There is a small white dot on the left side of the chip. <p>Detail photograph of NAND circuit in Samsung Galaxy S21 Ultra 5G</p>

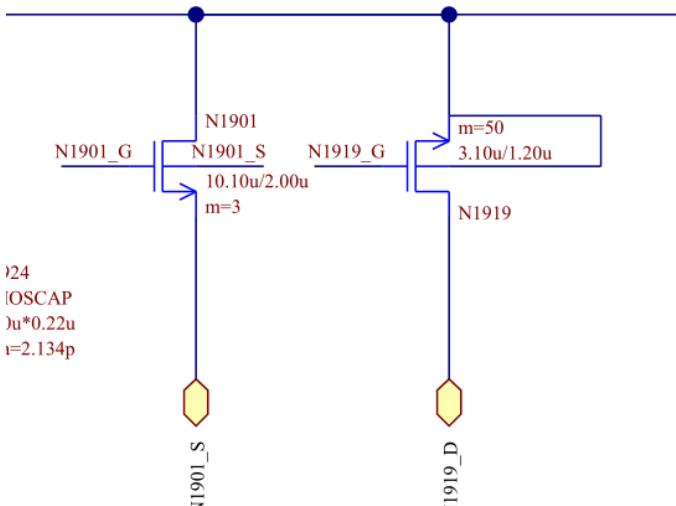
Claim 1	Accused Products
	 A high-magnification photograph of a portion of a NAND circuit. The image shows a dense array of horizontal and vertical metal lines, with a large, irregularly shaped purple polygon highlighting a specific region of the circuit. The overall structure is rectangular with various internal components and connections.
	 A photograph of a portion of a NAND circuit, showing a series of vertical columns of memory cells. Each column is composed of multiple horizontal lines, likely representing the word lines and bit lines of a NAND cell. The cells are arranged in a grid pattern, with a dark border around the entire array.

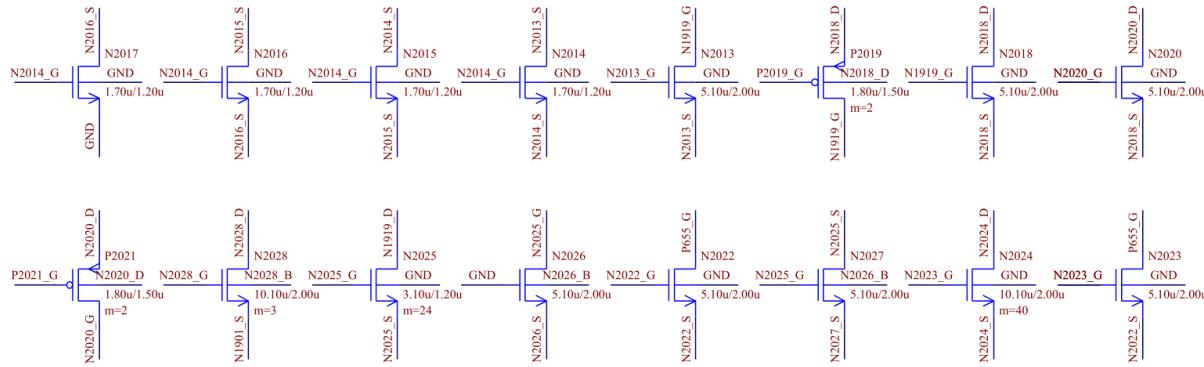
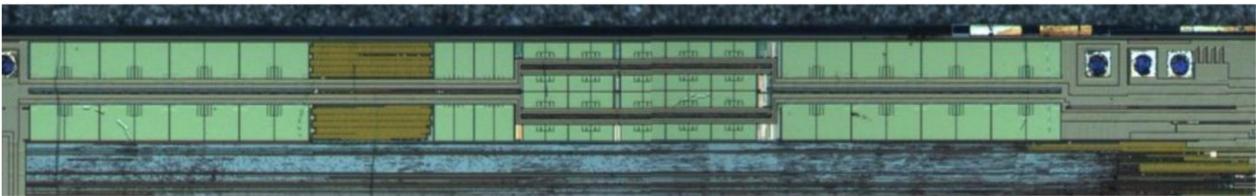
Claim 1	Accused Products
	 <p>Detail photograph of portion of NAND circuit from Samsung Galaxy S21 Ultra 5G</p>  <p>Schematic of NAND charge pump circuit from Samsung Galaxy S21 Ultra 5G</p> <p>The schematic shows a four-stage charge pump circuit. Stage 1 (CHARGE PUMP_1) has a gain of 2.0 and is controlled by P102, N192, and N193. Stage 2 (CHARGE PUMP_2) has a gain of 2.4 and is controlled by P103, N194, and N195. Stage 3 (CHARGE PUMP_3) has a gain of 2.1 and is controlled by P104, N196, and N197. Stage 4 (CHARGE PUMP_4) has a gain of 2.1 and is controlled by P105, N198, and N199. The circuit includes various transistors (M100 to M105, N190 to N199), capacitors (C101 to C105), and resistors (R101 to R105). The output of the fourth stage is connected to the NAND circuit.</p>
<p>[1a] a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;</p> <p><i>See, e.g.:</i></p>	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, the NAND charge pump circuit of the Samsung Galaxy S21 Ultra 5G comprises the pumping circuit shown below.</p>

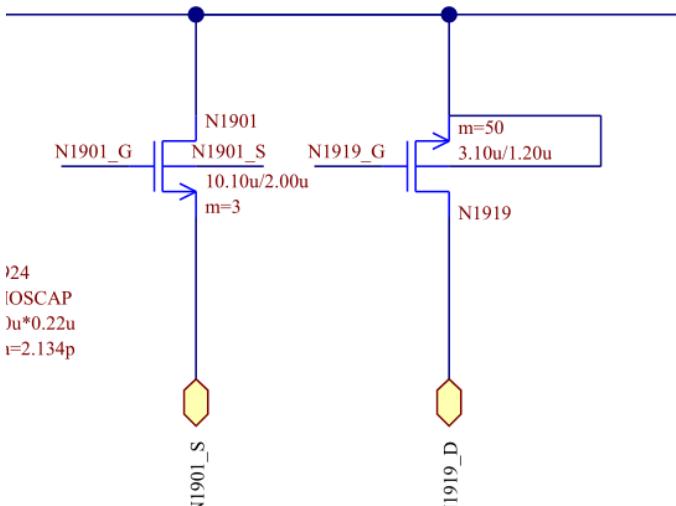
Claim 1	Accused Products
	 <p>Detail photograph of portion of NAND circuit from Samsung Galaxy S21 Ultra 5G</p>

Claim 1	Accused Products
	 <p>Schematic of charge pump circuit from Samsung Galaxy S21 Ultra 5G</p>

Claim 1	Accused Products
	 <p>Detail schematic of a portion of CHARGEUPM_2</p>

Claim 1	Accused Products
	 <p>Detail from schematic of charge pump circuit from Samsung Galaxy S21 Ultra 5G showing loads selectively coupleable to the output of the pumping circuit</p>

Claim 1	Accused Products
	 <p>Detail from schematic of charge pump circuit from Samsung Galaxy S21 Ultra 5G showing loads selectively coupleable to the output of the pumping circuit</p>
<p>[1c] a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit</p> <p><i>See, e.g.:</i></p>  <p>Detail photograph of portion of NAND circuit from Samsung Galaxy S21 Ultra 5G</p>	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p>

Claim 1	Accused Products
	 <p>Detail from schematic of charge pump circuit from Samsung Galaxy S21 Ultra 5G showing loads selectively coupleable to the output of the pumping circuit</p>

Claim 2

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref}).</p> <p><i>See evidence and explanation for claim element [1a], <i>supra</i>.</i></p>

Claim 2	Accused Products
(Vcfra) is greater than or equal to a reference voltage (Vref).	

Claim 3

Claim 3	Accused Products
3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).</p> <p><i>See evidence and explanation for claim element [1a] and claim 2, <i>supra</i>.</i></p>

Claim 6

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p>

Claim 6	Accused Products
<p>second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p>	<p><i>See evidence and explanation for claim element [1c] supra.</i></p>

Claim 7

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See evidence and explanation for claim element [1c] supra.</i></p>

Claim 8

Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second</p>

Claim 8	Accused Products
having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.	terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor. <i>See</i> evidence and explanation for claim element [1c] <i>supra</i> .